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(57) Abstract :

Disclosed herein is a system to design fast and energy efficient memory built-in self-test architecture using verification and logic (100) comprises a memory array (102) to test for faults. The system includes a pseudo-random pattern generator (104) for generating test patterns. The system also includes a deterministic pattern generator (106) for generating specific fault detection patterns. The system also includes a test controller (108) configured to control the application of test patterns to the memory array. The system also includes a state machine (110) to manage test sequences. The system also includes a clock gating unit (112) to reduce power consumption during testing. The system also includes a response analyzer (114) configured to analyze the output response of the memory array to the applied test patterns. The system also includes a signature analyzer (116) for compressing test responses into a signature.

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